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EXAMINER	
ECKERT II, GEORGE C	

ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
08/903,453	Forbes et al.
Examiner	**Art Unit**
George C. Eckert II	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *9/23 and 10/29/02*.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *2, 3, 24-28, 41-48, 50-52, and 65-68* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *2, 3, 24-28, 41-48, 50-52, and 65-68* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). *37 & 40*
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Amendment

1. Applicant's response and supplemental response dated September 23, 2002 and October 29, 2002 respectively have been entered of record. Claims 2, 3, 24-28, 41-48, 50-52 and 65-68 are pending.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 2, 3, 24-28, 41-48, 50-52 and 65-68 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 11-18, 23, 24, 28, 32-37, 40, 48, 62, 67 and 69 of co-pending Application No. 08/902,843. Although the conflicting claims are not identical, they are not patentably distinct from each other because the present invention and co-pending Application no. 08/902,843 disclose a transistor having:

a source and a drain separated by a channel supported by a semiconductor substrate;

a floating gate formed between the source and the drain above the channel and separated by an insulative amorphous carburized silicon layer;

a control gate formed adjacent to and insulated from the floating gate;

wherein the transistor is part of a memory cell comprising a capacitor.

Further, stacked capacitors are well known and widely used in memory devices.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 U.S.C. § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 2, 3, 24-28, 41-48, 50-52 and 65-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakata et al., *Amorphous silicon/amorphous silicon carbide heterojunctions applied to memory device structures*, Electronics Letters, April 28, 1994, Vol. 30, No. 9 (of record), in view of JP 8-255878 to Sugita et al. (of record) and Burns et al., *Principles of Electronic Circuits* (of record).

With regard to claims 2, 3, 24, 45, 46, 48, 50, 52, and 68, Sakata et al. teach in figure 1 the formation of an insulative layer of amorphous silicon carbide, shown as the a-SiC:H (graded)

layer, formed on top of a substrate which is crystalline silicon (c-Si) that can be p-type (see *Sample Preparation*);

a floating gate formed of amorphous silicon, shown as the a-Si:H layer, formed above the amorphous silicon carbide insulator,

a second insulative layer of amorphous silicon carbide, shown as the a-SiC:H layer, formed above the a-Si:H floating gate, and

a control gate shown as metal in figure 1 and later taught as aluminum (see *Sample Preparation*).

And though Sakata et al. teach that the above structure "can be applied to floating-gate memory devices[,]" Sakata et al. do not teach the structure further comprising a source region, a drain region, or a channel region therebetween. However, such regions are taught by Sugita et al. Specifically, Sugita et al. teach, with reference to figure 1, a floating gate memory device comprising:

an N+ type source region 2 and an N+ type drain region 3 (see page 11, paragraph 0032 of the translated reference which states that the source and drains 2 and 3 are n+ type);

the source and drain regions formed in a p-type silicon substrate (see page 2 of the translated reference which lists the reference numerals and corresponding elements and shows that numeral 1 represents a p-type silicon substrate);

a channel region between the source and drain regions in the substrate (though the channel region is not numbered, it is inherent that there exists a channel region between the source and

drain of a transistor, see *Principles of Electronic Circuits*, pp. 382-83 shows an n+ source and an n+ drain in a p-type substrate and refers to the device as one comprising an "n-channel");

a floating gate 6 (see page 3 of the translated reference and the list of elements which labels numeral 6 as a polysilicon floating gate) which is formed above and insulated from the substrate;

a control gate 8 formed above the floating gate and separated from the floating gate by a dielectric layer 7 (again, see the list of elements on page 3 of Sugita et al. where element 8 is labeled a control gate and element 7 is listed as SiO_2, a known, inherent insulator).

Sakata et al., Sugita et al. and Burns et al. are combinable because they are from the same field of endeavor, which field is the formation of floating gate devices. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form a source region, drain region and channel region in the device of Sakata et al. The motivation for doing so is that the source, drain and channel regions allow individual floating gate devices to be formed in an array. That is, by forming source and drain regions having the floating gate stack therebetween, a plurality of floating gate devices can be formed in one substrate and yet be individually written and erased by the use of the source, drain and channel regions. The use of the source/drain/channel regions for such programming is well known in the art. For example, Burns et al. explicitly teach such programming steps in the paragraph bridging pages 382-83. Furthermore, Sugita et al. generally teach this integration concept in paragraphs 0001 - 0005 of

the translated reference. Therefore, it would have been obvious to combine Sakata et al. with Sugita et al. and Burns et al. to obtain the invention of claims 2, 3, 24-28, 41-48, 50-52, & 65-68.

Regarding the use of polysilicon as the material for the control gate, Sakata et al. indicate that the control gate is formed of aluminum while Sugita et al. are silent as to the material for their control gate. However, Burns et al. teach on page 382 that control gates (or, as there labeled, select gates) are typically formed of polysilicon. Even beyond the teaching of Burns et al., the use of polysilicon as a control gate is considered well known in the art. There are several advantages of using polysilicon as a control gate, for example, polysilicon can be doped to a low resistivity and is able to withstand higher temperatures so that it is unaffected during subsequent annealing steps. As such, it is considered obvious to form the control gate of Sakata et al. from polysilicon.

As to the method of formation of the insulation layer between the floating gate and the substrate from silicon carbide, Sakata et al. teach or in the alternative make obvious such a structure. The limitation that the amorphous carburized silicon is *grown* on the substrate is taught or in the alternative obvious over Sakata et al. In support of the process term *grown*, it is noted that applicant's *growth* method is a deposition (specification p. 6, lines 3-4). Sakata et al. also teach a deposition method (see *Sample preparation*). As such, Sakata et al.'s deposition process anticipates the growth process limitation as instantly claimed.

In the alternative, and with further regard to the limitation where the *growth* process is further limited to be a microwave PECVD, limitations in the instant claims as to the process by which the final product is achieved do not distinguish over that taught by Sakata et al. That is,

such limitations are product by process limitations. Note that a "product by process" claim or limitation is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that, once a product appearing to be substantially identical is found and a rejection is made, the burden shifts to the applicant to show an unobvious difference based on the claimed process steps. MPEP §2113. Instantly, because no evidence was proffered by applicant as to patentability based on the added process limitations, the burden remains with applicant to do so.

4. Claims 2, 3, 24-28, 41, 45, 46, 50, 65 and 68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lott et al., *Charge Storage in InAlAs/InGaAs/InP Floating Gate Heterostructures* (from IDS, Paper #40) in view of Sakata et al., *Amorphous silicon/amorphous silicon carbide heterojunctions applied to memory device structures* (of record).

Lott et al. teach in figure 2 a floating gate device having an N+ source and an N+ drain separated by a channel ("sense channel") which source/drain and channel form a substrate, a gate

supported by the substrate and extending between the source and drain above the channel; and a barrier on the channel and between the channel and the gate. Lott et al. also teach in figure 2 a floating gate and control gate insulated from each other. However, Lott et al. do not teach that the barrier layer is an insulative amorphous layer of carburized silicon grown on the channel or that the substrate is p-type Si.

Sakata et al. teach, with reference to figure 1, a device in which an amorphous layer of carburized silicon (a-SiC:H) is formed directly on a substrate made of silicon (c-Si). Sakata et al. further teach that the substrate may be p-type (page 688, col. 2, under *Sample Preparation*).

As to the method of formation of the insulation layer between the floating gate and the substrate from silicon carbide, Sakata et al. teach or in the alternative make obvious such a structure. The limitation that the amorphous carburized silicon is *grown* on the substrate is taught or in the alternative obvious over Sakata et al. In support of the process term *grown*, it is noted that applicant's *growth* method is a deposition (specification p. 6, lines 3-4). Sakata et al. also teach a deposition method (see *Sample preparation*). As such, Sakata et al.'s deposition process anticipates the growth process limitation as instantly claimed.

In the alternative, and with further regard to the limitation where the *growth* process is further limited to be a microwave PECVD, limitations in the instant claims as to the process by which the final product is achieved do not distinguish over that taught by Sakata et al. That is, such limitations are product by process limitations. Note that a "product by process" claim or limitation is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ

15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that, once a product appearing to be substantially identical is found and a rejection is made, the burden shifts to the applicant to show an unobvious difference based on the claimed process steps. MPEP §2113. Instantly, because no evidence was proffered by applicant as to patentability based on the added process limitations, the burden remains with applicant to do so.

Lott et al. and Sakata et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the floating gate memory device of Lott et al. using the silicon based materials taught by Sakata et al., specifically the amorphous silicon carbide insulating layer on the silicon substrate. The motivation for doing so, as is taught by Sakata et al., is that devices using a III-V heterojunction suffer excessive leakage current which is reduced by using the silicon based materials. Therefore, it would have been obvious to combine Lott et al. with Sakata et al. to obtain the invention of claims 2, 3, 24, 45, 46, 50, 52 and 68.

5. Claims 42, 43, 47, 48, 51, 52, 66 and 67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lott et al. in view of Sakata et al. and Burns et al. (of record). Lott et al. and Sakata et al. teach the structure of the instant claims but did not teach that control gate was made of polysilicon. Burns et al. teach on page 382 that control gates (or, as there labeled, select gates) are typically formed of polysilicon.

Lott et al. and Sakata et al. are combinable with Burns et al. because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the device of Lott et al. and Sakata et al. having a polysilicon control gate electrode as taught by Burns et al. The motivation for doing so is that there are several advantages of using polysilicon as a control gate, for example, polysilicon can be doped to a low resistivity and is able to withstand higher temperatures so that it is unaffected during subsequent annealing steps. As such, it is considered obvious to form the control gate of Lott et al. and Sakata et al. from polysilicon. Therefore, it would have been obvious to combine Lott et al., Sakata et al. and Burns et al. to obtain claims 42, 43, 47, 48, 51, 52, 66 and 67.

Response to Arguments

6. Applicant's arguments filed October 29, 2002 have been fully considered but they are not persuasive. As noted above, the rejection of all claims as obvious over Sakata in view of Sugita and Burns is maintained. As such, applicant's arguments to that rejection are here considered but are not persuasive.

Applicant first argues that there is no suggestion to combine Sakata with Sugita and quotes Sakata's statement that "the present structure can be used as a component of dynamic random access memories (DRAMs) [4] at room temperature." Applicant has also supplied two references - Qian and Rahman - which show memory devices purportedly configured without a source or drain. The implication of these arguments and secondary references seems to be that the device of Sakata cannot be formed with a source and drain. However, that conclusion cannot be supported. Specifically, though Sakata do state that their invention may be used in a DRAM, that does not undermine or negate its use in a floating gate structure, which structure does have sources and drains. Especially in light of Sakata's statement; "we propose and experimentally confirm that the HJ structure of Fig. 1 can be applied to ***floating gate memory devices***." (***Emphasis added***).

As to the use of the Sakata structure in a floating gate device, applicant appears to concede Sakata's statement that their structure *can* be used in such a device. However, applicant argues that an actual implementation of the Sakata teaching in a floating gate device will not result in the instantly claimed structure. Specifically a source and drain formed *in* the substrate. For support, applicant has provided the Lott article *Anisotropic Thermionic Emission of Electrons Contained in GaAs/AlAs Floating Gate Device Structures*. This article will be referred to as Lott-1. The Lott-1 reference is included because it, like Sakata, refers to an article by Capasso. The Capasso article is important because it, like Sakata, taught a floating gate device; however, it, unlike Sakata, does make mention that a floating gate device has sources and drains.

The Capasso article was thus used as yet further evidence that floating gate devices use sources and drains. Unfortunately, Capasso did not provide a figure showing the layout of the sources and drains in relation to the substrate.

Applicant appears to have answered the structural question by finding the Lott-1 article which, like Sakata, makes reference to the Capasso paper, but additionally shows a structure of a floating gate device. More importantly, Lott-1 says its structure "has a vertical structure similar to that of Capasso et al." As such, the Capasso structure must also have been, and probably was, the same type of vertical structure as shown by Lott-1. From this, applicant concludes that the statement by Sakata - that their device can be applied to floating gate devices - must have contemplated a final structure similar to Lott-1's which has the source and drain above the substrate and in fact above a superlattice. However, such argument is not found persuasive. First of all, Sakata teaches a device based in silicon while Capasso and Lott-1 contemplate devices of III-V material which have different structures. Secondly, even assuming *arguendo* that the device of Sakata is limited to the same structure as that of a III-V device, such III-V structures *can* be formed having the source and drain in the substrate as instantly claimed. Finally, tying the structure of Sakata to that taught by Lott-1 too narrowly reads the Sakata disclosure. The second point will be addressed first.

As to the formation of a III-V floating gate device having the source and drain in the substrate, Applicant has provided a second article by Lott entitled *Charge Storage in InAlAs/InGaAS/InP Floating Gate Heterostructures* which will be referred to as Lott-2 (which is

the same reference as used in the new rejections of the instant claims). As Lott-2 clearly shows in figure 2, a III-V floating gate structure has been formed. Importantly however, the source and drain regions are clearly shown as formed on either side of the sense channel region, are formed of the same material, and are located in the lowermost portion of the device (i.e. below the barrier/insulator, floating gate and control gate). The source and drain regions are N+ doped regions in the substrate formed of InGaAs, which substrate also includes the undoped sense channel formed of InGaAs. As such, even if the teaching of Sakata were limited to application in structures based on III-V devices, Lott-1 cannot be construed as limiting the teaching to only one structure wherein the source and drain are formed above a superlattice. Lott-2 clearly teaches a III-V structure wherein the source and drain are formed in the substrate.

However, Sakata's teaching is to a device based in silicon, as is Sugita's. Such a device, as is clearly shown by Sugita, has the source and drain formed *in* the silicon substrate. Moreover, the channel region is also formed in the substrate, of the same material, and located between the source and drain. Note again, as made clear in the above rejection, that although Sugita does not expressly state the word "channel," such a channel is inherent between the source and drain as taught by Burns. Furthermore, it is not only Sugita that teaches a Si based floating gate wherein the source and drain are formed in the silicon substrate, but also Burns, Ng and several other (essentially all) references of record.

But even if there were found some reference which taught a silicon based floating gate memory device in which the source and drain were somehow formed above a superlattice and

above the floating gate, it would not defeat the rejection. This is because it is the source and drain of Sugita which are motivated for use in the substrate of Sakata. That is, motivation is found - and was established in the rejection - to use a source and drain region in the Si substrate of Sakata. The use of the source and drain allows the device of Sakata to be formed in an array.

Finally, the whole basis of undermining the combination of Sakata and Sugita and limiting any application of Sakata to a 'source/drain above superlattice' structure as taught by Lott-1, is solely the statement by Sakata that "Capasso et al. reported *similar memory devices* based on AlGaAs/GaAs HJ." (*Emphasis added*). But this is too narrow a reading of that statement by Sakata. The phrase "similar memory devices" does not carry with it the implication that the *structures* are absolutely the same. Rather, "similar memory devices" merely implies that the devices exploit band-gap features of their respective materials in order to store charge. Note Sakata's *Abstract* - ". . .proposed and experimentally confirmed that band-engineered amorphous silicon . . ."; Lott-1's first sentence -". . .charge storage in quantum wells of III-V. . ."; Lott-2's second sentence under *Introduction* - "Charge was stored in a potential well. . ."; and finally Capasso's *Abstract* ". . .using an AlGaAs graded-gap barrier." It is the exploitation of band engineering principles to store charge that makes these memory devices similar, rather than a requirement that they have the same structure.

Lastly, applicant argues that based on the structural dissimilarities between Lott-1 and Sugita - specifically the probable differences in operating principles - Sugita can not be combined with Sakata. The reason being that the devices of Sakata and Sugita would also probably operate

differently. However, for the reasons discussed in the previous Office action (Paper No. 35, *Response to Arguments*, beginning at page 11) this argument is not persuasive.

In all, the arguments here presented are not persuasive. The above rejection of the outstanding claims over Sakata and Sugita combined with Burns is a *prima facie* showing of obviousness and the rejection is therefore maintained.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. McElroy is cited for teaching the use of sources and drains to program a floating gate device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George C. Eckert II whose telephone number is (703) 305-2752.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Eddie Lee can be reached on (703) 308-1690. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

GCE
January 14, 2003

GEORGE ECKERT
PRIMARY EXAMINER